SLAVE-LESS EDGE-TRIGGERED FLIP-FLOP

ABSTRACT

An edge-triggered flip flop includes a clocking portion having first and second transistor stacks that are coupled to first and second storage nodes of a memory element, respectively. In at least one embodiment, a clock signal is applied to an input of at least one transistor in each stack and a delayed and possibly inverted version of the clock signal is applied to an input of at least one other transistor in each stack to clock new data into the memory element.